MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2018/2019

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

13 OCTOBER 2018
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 6 pages with 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_p = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_p = 0.69\, R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Figure Q1 shows a simple diode model with $V_{D(on)} = 0.7$ V.

(i) Determine current, (I_D) value of the circuit. [4 marks]

(ii) Reverse the polarity of the diode in Figure Q1(a), calculate the new I_D value. [2 marks]

(iii) Based on the new value calculated in (ii), discuss the main function of a diode. [2 marks]

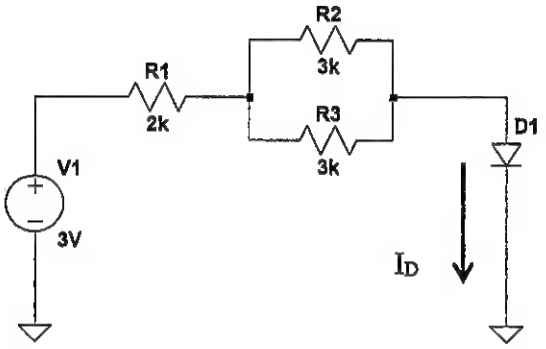

Figure Q1

(b) An NMOS transistor has aspect ratio W/L = 5/2 which is operating with $V_{SB} = 1.6$ V, $V_{GS} = 2$ V and $V_{DS} = 3$ V. For a minimum sized NMOS transistor the given threshold voltage is, $V_{T0} = 0.43$ V, $-2\varphi_F = 0.8$ V, body effect coefficient, $\gamma = 0.4\ \sqrt{V}$ and $k_n' = 115\ \mu A/V^2$. Determine the mode of operation and the drain current, I_D for this transistor.

[8 marks]

(c) For a cut-off region MOS transistor with given values:
Width, W = 15 μm, length, $L_{eff} = 1.5$ μm, and oxide thickness of 50 nm and $\varepsilon_{ox} = 3.5 \times 10^{-13}$ F/cm..

(i) Compute the oxide capacitance, C_{ox} and total capacitance, C_{gc}. [4 marks]

(ii) If the transistor operates in triode region, describe the change in the transistor structure.

[2 marks]

(d) An ideal transistor gives several second-order effects. Explain the secondary effect of CMOS latch-up and propose a solution to minimize the effect.

[3 marks]

Continued...

Question 2

(a) Based on a chain of inverters,

(i) Describe the regenerative property, including a sketch of the signals (V_0, V_1, V_2, ..) from the chain of inverters. [6 marks]

(ii) Explain the condition for a circuit to be regenerative. [2 marks]

(b) Given the function F below:

$$Y = (AB) + C$$

(i) Design a static CMOS gate realization of this function F with minimum transistor count. The input and inverted input ports are available for implementation. [6 marks]

(ii) From the design in Part (i), compute the W/L ratios of the transistors so that the output resistance is the same as that of an inverter with $(W/L)_{NMOS} = 2$ and $(W/L)_{PMOS} = 3$. [4 marks]

(c) Figure Q2 shows one of the astable multivibrators, the voltage controlled oscillator (VCO).

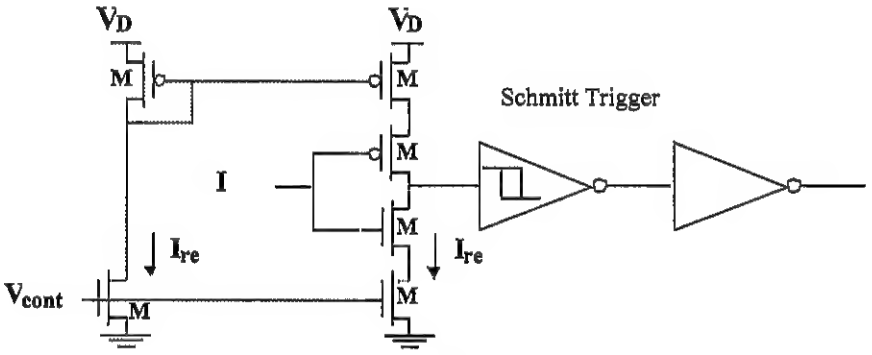

Figure Q2

(i) Describe the operation of the VCO, including the Schmitt Trigger. [5 marks]

(ii) Discuss the advantage it has compared to relaxation oscillator. [2 marks]

Continued...

Question 3

(a) Referring to Figure Q3(a) below, design the ECL OR/NOR gate of the circuit. It has two inputs. The desired collector currents are I_{R1} = 1 mA and V_{EE} = -5 V. At logic high, V_{OR} = -0.7 V, V_{NOR} = -1.5 V and $V_a = V_b$ = -0.7 V. Assume V_{BE} = 0.7 V and β = 50. [11 marks]

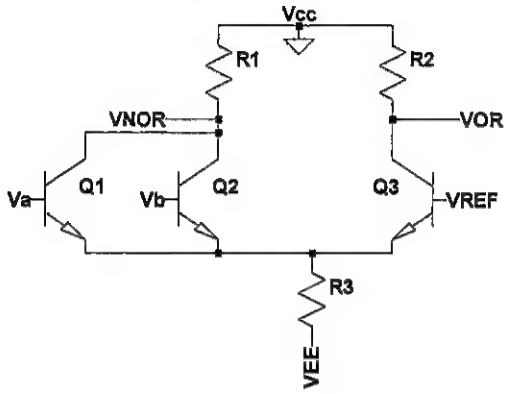

Figure Q3(a)

(b) Referring to Figure Q3(b), a TTL NAND circuit is shown.

(i) Modify (or re-design) the circuit in Figure Q3(b) to become Schottky TTL NAND gates. [4 marks]

(ii) Compare the advantage of the modified design in (i) with the circuit in Figure Q3(b), and critic the effects of Schottky diode especially on noise margin. [5 marks]

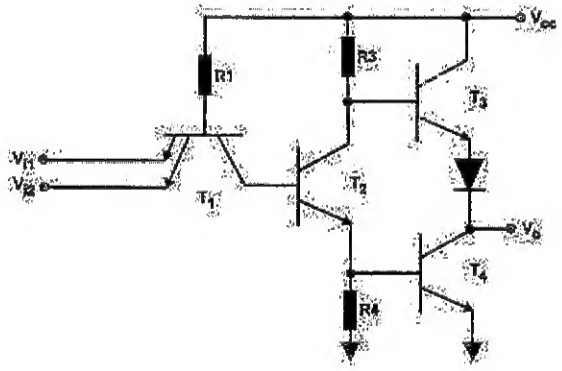

Figure Q3(b)

(c) In practice, the load of a logic gate is another logic gate. Describe FIVE requirements of interfacing of different logic gates. [5 marks]

Continued...

Question 4

(a) Implement the following functions using static CMOS gates:

$$Y = \overline{A.B + C}$$

[6 marks]

(b) Based on the circuit implemented in Part (a), determine the dynamic power consumption, P_{dyn} of the circuit, assuming that the load capacitance, C_L = 20 fF, voltage supply, V_{DD} = 3 V and clock frequency, f_{clk} = 200 MHz. Assume that the input signals are random.

Hint: Use a truth table.

[9 marks]

(c) Figure Q4 shows the Normalized Power as a function of Technology Node.

(i) Based on this Figure Q4, comment on the graph. [4 marks]

(ii) Recommend THREE methods to reduce power consumption. [6 marks]

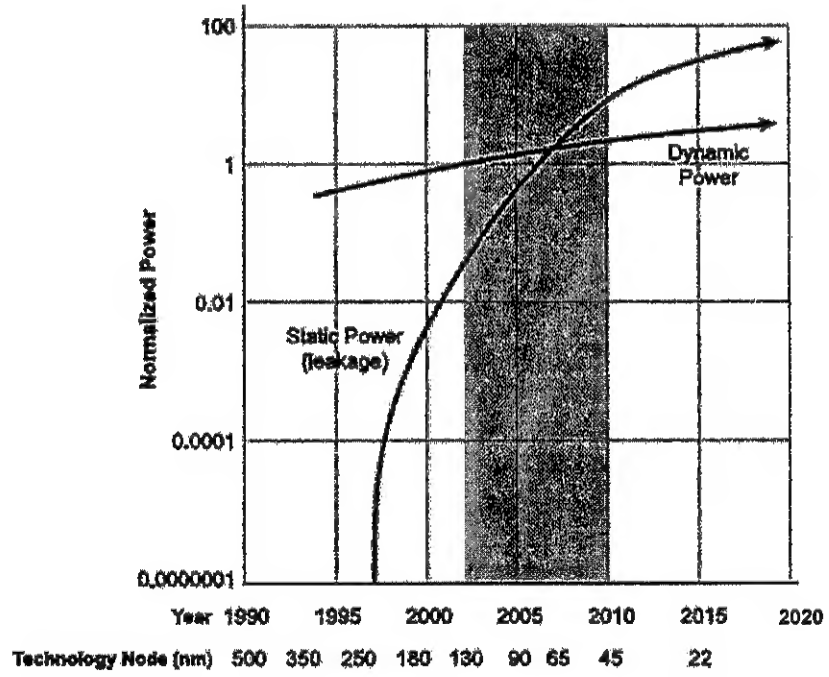

Figure Q4

End of Paper